



UNITED STATES PATENT AND TRADEMARK OFFICE

cen

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,004	02/08/2002	Woo Young So	1514.1010	6442

49455 7590 10/31/2006

STEIN, MCEWEN & BUI, LLP
1400 EYE STREET, NW
SUITE 300
WASHINGTON, DC 20005

EXAMINER

SEFER, AHMED N

ART UNIT	PAPER NUMBER
----------	--------------

2826

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/068,004

Applicant(s)

SO ET AL.

Examiner

A. Sefer

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 October 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 12, 14-16, 22 and 24-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 12, 14-16, 22 and 24-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. The amendment filed October 5, 2006 has been entered and no new claims have been added.

Priority

2. Submission of the translation of the foreign language application (KR 2001-10842) is acknowledged. Therefore, Chang et al. (US PG-Pub 2002/0153527) is not available as a prior art.
3. The indicated allowability of claims 15, 16, 22 and 24-28 is withdrawn in view of the newly discovered reference(s) to Yamazaki et al ("Yamazaki") US PG-Pub 2004/0041190 and Zhang ("Zhang") US PG-Pub 2002/0105033. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 12, 14-16, 26 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al ("Yamazaki") US PG-Pub 2004/0041190.

Yamazaki discloses in figs. 1-7 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer 602 formed over said substrate having end portions; a first insulating layer 603 disposed on said semiconductor layer so as to expose ones of the end portions of said

Art Unit: 2826

semiconductor layer; a gate electrode 604 formed over said first insulating layer; a capping layer 605 formed over said gate electrode; spacers 608/701 formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer; high-density source and drain regions 609/610 formed at the ends of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate electrode and the capping layer; low-density source and drain regions 611 having a same conductivity as high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high density source and drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions under said spacers; and source and drain electrodes 614/615 which respectively contact said high density source and drain regions without contact holes -- note that contact holes which might have been formed previously do not exist in the final structure as they have been filled with electrode materials.

Regarding claim 14, Yamazaki discloses said first insulating layer, said capping layer and said spacer are of an oxide.

Regarding claims 15 and 16, Yamazaki discloses a silicide layer being formed between said source electrode and said high density source region and a silicide 704 between said drain electrode and said high density drain region; wherein said silicide layer comprise refractory metal (**as in claim 16**).

Regarding claim 26, Yamazaki discloses said high-density source and drain regions and said low-density source and drain regions extend through an entire thickness of said semiconductor layer.

Art Unit: 2826

Regarding claim 28, Yamazaki discloses said high-density source and drain regions being formed at entireties of the end portions of said semiconductor layer exposed beyond said spacers; and wherein said low-density source and drain regions having a same conductivity as said high-density source and drain regions are formed at entireties of regions of semiconductor layer entirely under said spacers between the gate electrode and the high-density source and drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers.

5. Claims 22, 24 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki.

Yamazaki discloses in figs. 1-7 an active matrix display device, comprising: a substrate; a semiconductor layer 602 having end portions formed over said substrate; a first insulating layer 603 formed over said semiconductor layer so as to expose one of the end portions of said semiconductor layer; a gate electrode 604 formed over said first insulating layer; a capping layer 605 formed over said gate electrode; spacers 608/701 formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer; high-density source and drain regions 609/610 formed at entireties of the end portions of said semiconductor layer exposed beyond said spacers; low-density source and drain regions 611 having a same conductivity as said high-density source and drain regions formed at entireties of off-set regions of said semiconductor layer entirely under said spacers, thereby said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers; source and drain electrodes 614/615 which respectively contact said high density source and drain regions -- note that contact holes which might have been formed previously do not exist in the final structure as they

Art Unit: 2826

have been filled with electrode materials; a planarization layer 349 having an opening portion which exposes a portion of one of said source and drain electrodes; and a pixel electrode 350 formed on the planarization layer, the pixel electrode contacting one of the second source and drain electrodes through the opening portion.

Regarding claim 24, Yamazaki discloses a silicide layer 704 being formed between said source electrode and said high density source region and a silicide 704 between said drain electrode and said high density drain region

Regarding claim 27, Yamazaki discloses said high-density source and drain regions and said low-density source and drain regions extend through an entire thickness of said semiconductor layer.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang ("Zhang") US PG-Pub 2002/0105033 in view of Yamazaki et al. USPN 5,568,288 ("Yamazaki '288").

Zhang discloses in figs. 10A-10F a thin film transistor (TFT), comprising: a substrate; a semiconductor layer 104 formed over said substrate having end portions; a first insulating layer 106 disposed on said semiconductor layer so as to expose ones of the end portions of said

Art Unit: 2826

semiconductor layer; a gate electrode 108 formed over said first insulating layer; a capping layer (upper portion of region 109) formed over said gate electrode; spacers (portions of region 109 on both sidewall portions of gate electrode 108) formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer; high-density source and drain regions 124n formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate electrode and the capping layer; low-density source and drain regions 114n/104f having a same conductivity as high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high density source and drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions under said spacers, but lacks anticipation of source and drain electrodes contacting high density source and drain regions without contact holes.

Yamazaki '288 discloses in figs. 21 and 22 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate having end portions; a gate electrode 107 formed over an insulating layer 103; and source and drain electrodes 102 which respectively contact high density source and drain regions 104/105 without contact holes.

Therefore, in view of Yamazaki '288, one having ordinary skill in the art at the time the invention was made would be motivated to modify Zhang's device by incorporating the teachings of Yamazaki so as to complete the thin film transistor as taught by Yamazaki '288.

Regarding claim 14, Zhang discloses said first insulating layer, said capping layer and said spacer are of an oxide.

Art Unit: 2826

8. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Yamazaki et al. US PG-Pub 2003/0207502 ("Yamazaki '502").

Yamazaki discloses (par. 4) the device structure as recited in the claim including an electro-optical device but does not specifically disclose an EL layer.

Yamazaki '502 discloses (par. 0343 and fig. 25) an organic electro-luminescence (EL) layer 4029 and a cathode electrode 4030 sequentially formed on a first predetermined area of a pixel electrode and on a second predetermined area of a planarization layer 4142.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Yamazaki '502 with Yamazaki so as to realize a high efficiency integrated device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

Art Unit: 2826

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ANS

October 22, 2006



A. Sefer
Patent Examiner
Art Unit 2826